Energy-based Method to Estimate the Partial Hard Turn-on Loss of Complementary SiC MOSFET from Experiment

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2024 IEEE Applied Power Electronics Conference and Exposition (APEC) | 979-8-3503-1664-3/24/$31.00 ©2024 IEEE | DOI: 10.1109/APEC48139.2024.10509333

***Abstract*—In a capacitor-assisted soft-switching converter, the zero-voltage turn-on (lossless) of the complementary MOSFET is lost at low values of load current, and it incurs a significant amount of turn-on loss. This phenomenon is termed as the partial hard turn-on, and it is a special case of soft-switching dynamics. Estimation of partial hard turn-on loss is essential for predicting light load efficiency of any soft-switched converter. However, direct experimental measurement is not accurate due to the presence of circuit parasitics. Also, it is difficult to measure waveforms of high-side devices due to high-frequency common mode voltage. This paper proposes an alternate energy-based method to estimate the partial hard turn-on loss of the complementary MOSFET using experimental data. This method is derived from the behavioral model through approximations. Although indirect, this method results in a simple and accurate estimation of partial hard turn-on loss from measured waveforms. The proposed energy-based technique is verified through behavioral simulation and experiment for a 39A, 1200V SiC MOSFET for a wide range of operating conditions.**

***Index Terms*—zero-voltage switching (ZVS), partial hard turn-on, soft-switching, loss, experiment, measurement, energy-based method, SiC MOSFET**

I. Introduction

Soft-switching converters (e.g., dual-active bridge (DAB)) can achieve higher switching frequency due to their reduced switching loss. SiC MOSFETs are a promising choice for these converters [1]. In such converters, hard turn-on transition is avoided, and turn-off losses dominate the total switching loss. External capacitance can be used to reduce both (dv/dt) and turn-off loss.

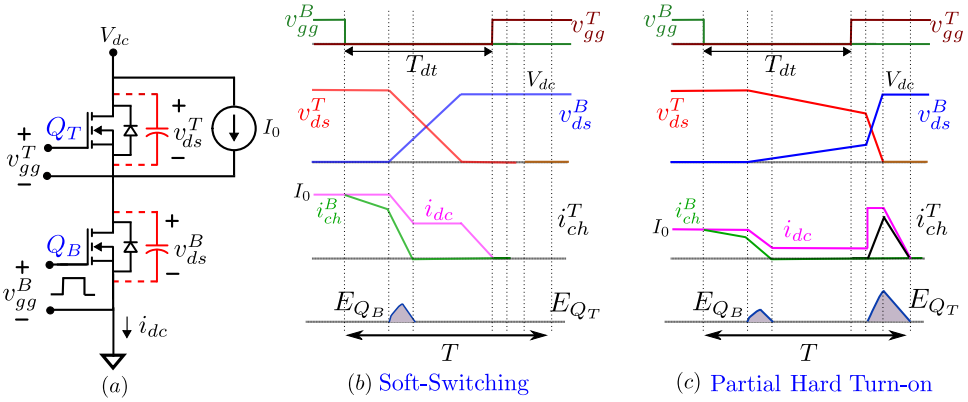
To understand the capacitor-assisted soft-switching dynamics, SiC MOSFETs (Q_B, Q_T) are considered in a half-bridge configuration (see Fig. 1(a)) with input dc voltage V_{dc} and output load current I_0. As Q_B is turned off, its drain-source voltage (v_{ds}^B) rises to V_{dc} and then its current (I_0) gets transferred to the body diode of Q_T. Hence, Q_T can now be turned on after a deadtime period (T_{dt}) at almost zero-voltage $(v_{ds}^T \approx 0)$, resulting in negligible turn-on loss of Q_T (see Fig. 1(b)). However, voltage rise is load current dependent, and at low load conditions, the voltage rise time of Q_B is significantly large. Now, due to finite deadtime, Q_T may turn on before its anti-parallel body diode conducts. Thus, Q_T may get turned on at substantial v_{ds}^T, resulting in a significant turn-on loss (see Fig. 1(c)). *This is known as the partial hard turn-on transition of* Q_T. Note: Q_B has a small overlap loss in both cases.

Estimation of switching losses is essential to determine the switching frequency of a power converter and to dimension the thermal system. Switching loss can be obtained experimentally through a widely used double-pulse test (DPT) by integrating the product of device current and voltage over a switching transition time. However, the measured loss can differ significantly from the actual loss of the device due to the presence of circuit parasitics (inductances and capacitances) [2]. Moreover, the measurement of high-side device waveforms is difficult due to the presence of high-frequency common-mode voltage. Among the other switching loss estimation methods, simulation (physics-based [3] and behavioral [4]) methods are accurate. However, they require expensive software packages, larger computation time, and experience convergence issues [5] and are therefore not preferred by design engineers. On the other hand, analytical models [2], [6]–[8] divide the switching transitions into multiple modes and employ suitable approximations to obtain a closed-form solution or a reduced-order model. Although simple and easy to code, they are less accurate compared to simulation-based approaches. An alternate energy-based switching loss estimation technique using experimentally measured data was earlier proposed for obtaining hard turn-on, hard turn-off, and soft-switching loss in [9]. However, partial hard turn-on loss was not addressed.

In this paper, an energy-based method is presented to estimate the partial hard turn-on loss of the complementary SiC MOSFET. It requires only the measurement of the active device's voltage and current waveforms, along with the load current waveform, to compute the loss. This method is derived from the behavioral model (which takes device parameters obtained from the datasheet and circuit parasitics as input) through suitable approximations. The proposed method is verified through experiment and simulation for a 39A, 1200V SiC MOSFET (LSIC1MO120E0080) from Littelfuse for a wide range of operating conditions.

II. Behavioral Model

The behavioral model for analyzing the partial hard turn-on dynamics is shown in Fig. 2(a) (circuit configuration in Fig. 1(a) redrawn with SiC MOSFET models and relevant



(a) (b) Soft-Switching (c) Partial Hard Turn-on

Fig. 1: (a) Half-bridge circuit (b) Soft turn-on waveforms (c) Partial hard turn-on waveforms

$$i_{ch}(v_{gs}, v_{ds}) = \begin{cases} 0, & v_{gs} < V_{th} \\ \dfrac{K_p K_f \left((v_{gs} - V_{th})\, v_{ds} - \left(\dfrac{P_{vf}^{y-1}}{y} \right) (v_{gs} - V_{th})^{2-y}\, v_{ds}^{y} \right)}{(1 + \theta(v_{gs} - V_{th}))}, & v_{gs} \geq V_{th} \quad v_{ds} < \left(\dfrac{v_{gs} - V_{th}}{P_{vf}} \right) \\ \dfrac{K_p\,(v_{gs} - V_{th})^2}{2(1 + \theta(v_{gs} - V_{th}))} & v_{gs} \geq V_{th} \quad v_{ds} > \left(\dfrac{v_{gs} - V_{th}}{P_{vf}} \right) \end{cases} \tag{1}$$

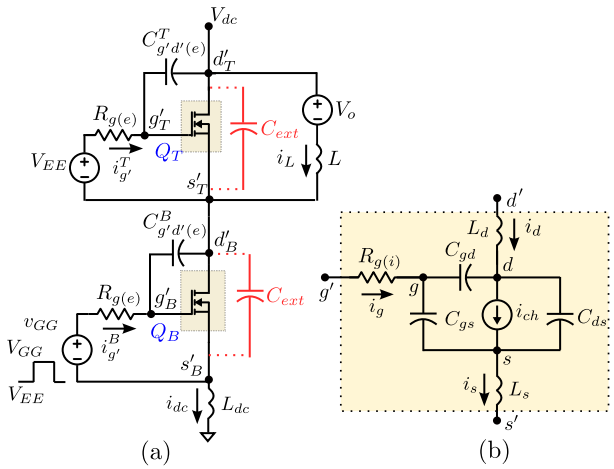


Fig. 2: (a) Circuit Configuration for partial hard turn-on analysis (b) Behavioral model of SiC MOSFET

parasitics). V_{dc} is the input DC bus voltage. Instead of a constant current sink model used in [8], this paper models the output inductive load as an inductor (L) in series with a voltage source (V_o). The model can accurately capture the turn-off switching transient waveforms for the entire load range, especially at light load conditions. C_{ext} represents the external drain-source capacitance required for minimizing turn-off loss at high load conditions.

The behavioral model of SiC MOSFETs (Q_B, Q_T) is shown in Fig. 2(b). It is modeled as three-terminal device (g', d', s') and consists of a dependent current source ($i_{ch}(v_{gs}, v_{ds})$), three dependent capacitors ($C_{gs}, C_{gd}(v_{dg}), C_{ds}(v_{ds})$), internal gate resistance $R_{g(i)}$ and lead inductances L_d, L_s. The detailed nonlinear models of i_{ch} and device capacitances are considered, as shown in (1)-(4). The parameters associated with these models ($K_p, K_f, V_{th}, P_{vf}, y, \theta, k_1 - k_9$) are extracted by curve-fitting the datasheet curves (shown in Table I). Moreover, these nonlinear voltage-dependent capacitors $C(v)$ can be replaced by their equivalent energy-related capacitance $C^{Er}(V_1, V_2)$ and charge-equivalent capacitance $C^{Q}(V_1, V_2)$ in the voltage interval $v \in (V_1, V_2)$ (see (5) and (6)).

$$C_{gd}(v_{dg}) = \begin{cases} C_{oxd} = \dfrac{k_1}{k_3}, & v_{dg} \in (-\infty, 0) \\ \dfrac{k_1}{\left(1 + \dfrac{v_{dg}}{k_2}\right)^{1/2} + k_3}, & v_{dg} \in [0, V_{td}) \\ \dfrac{k_4}{\left(1 + \dfrac{v_{dg} - V_{td}}{k_5}\right)^{1/4}}, & v_{dg} \in [V_{td}, \infty) \end{cases} \tag{2}$$

$$C_{ds}(v_{ds}) = \frac{k_6}{\left(1 + \dfrac{v_{ds}}{k_7}\right)^{1/2}} \tag{3}$$

$$C_{oss}(v_{ds}) = \frac{k_8}{\left(1 + \dfrac{v_{ds}}{k_9}\right)^{1/2}} \tag{4}$$

$$C^{Er}(V_1, V_2) = \frac{2}{V_2^2 - V_1^2} \int_{V_1}^{V_2} v C(v) dv \tag{5}$$

$$C^{Q}(V_1, V_2) = \frac{1}{V_2 - V_1} \int_{V_1}^{V_2} C(v) dv \tag{6}$$

$v_{d's'}^B(t)$ and $i_{dc}(t)$ are the waveforms obtained through experimental measurement as it is not possible to access devices'

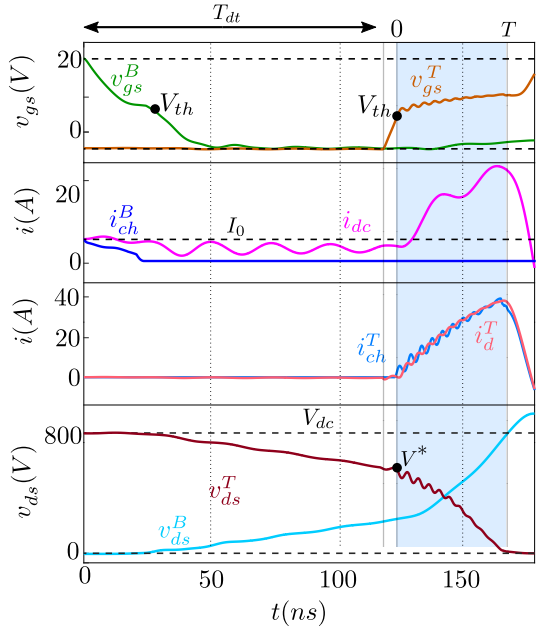


Fig. 3: Simulated Waveforms $[800V, 5A, 1000pF, 3\Omega]$

internal nodes (g, d, s). In conventional loss measurement using DPT, switching loss is calculated using (7) where T is the transition time. In contrast, the actual loss inside the MOSFET channel during the switching transition can be estimated as (8), which requires information about the time evolution of $i_{ch}^T(t)$ and $v_{ds}^T(t)$. However, due to fast switching transients of SiC MOSFET, the impact of parasitics is significant. So $i_{ch}^T(t)$ and $v_{ds}^T(t)$ can not be measured experimentally, and there can be a significant difference between the actual loss E and the measured loss E' [9].

$$E'_{Q_T} = \int_0^T v_{d's'}^T(\tau) i_d^T(\tau) d\tau \tag{7}$$

$$E_{Q_T} = \int_0^T v_{ds}^T(\tau) i_{ch}^T(\tau) d\tau \tag{8}$$

III. Energy-based method for Estimating Partial Hard turn-on loss

The behavioral model discussed in Section II is simulated in MATLAB/Simulink, and the important waveforms are shown at the operating condition $[V_{dc} = 800V, I_0 = 5A, C_{ext} = 1000pF, R_{g(e)} = 3\Omega]$ in Fig. 3. It can be observed that the partial hard turn-on loss in the complementary device Q_T occurs after the deadtime period (T_{dt}) when it gets turned at substantial drain-source voltage $v_{ds}^T = V^*$ (shown in shaded region in Fig. 3). Therefore, to estimate the loss, only the shaded region is analyzed, and the equivalent circuit is shown in Fig. 4. The device parameters $(R_{g(i)}, i_{ch}, C_{gs}, C_{gd}, C_{ds})$ are obtained from the datasheet. The circuit parasitics (inductances - L_d, L_s, L_{dc}, and capacitance - $C_{g'd'(e)}^T, C_{g'd'(e)}^B$) are obtained from the experiment [10].

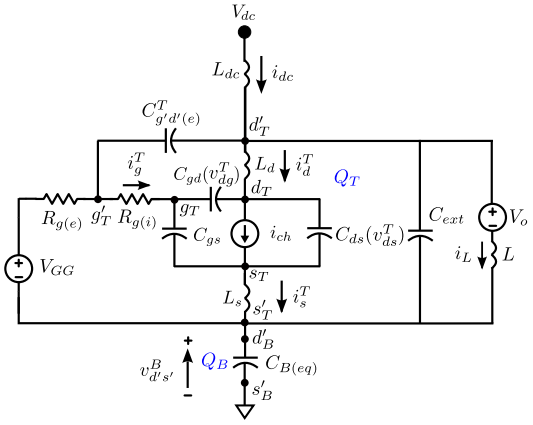


Fig. 4: Equivalent circuit of Partial Hard turn-on dynamics

$$i_{dc} \approx i_{ch}^T + C_{T(eq)} \frac{d}{dt} v_{ds}^T + i_L \tag{9}$$

$$i_{dc} \approx C_{B(eq)} \frac{d}{dt} v_{ds}^B \tag{10}$$

$$V_{dc} \approx v_{ds}^T + v_{ds}^B + (L_d + L_s) \frac{di_{dc}}{dt} \tag{11}$$

$$v_{ds}^T = V_o + L \frac{i_L}{dt} \tag{12}$$

Before $t = 0$, Q_B has turned off $(i_{ch}^B = 0)$. So, it is modeled as an equivalent output capacitance $C_{B(eq)}$[1]. Due to insufficient deadtime at low values of load current, the Q_T turns on before the end of the voltage transition period (i.e., $v_{ds}^T > 0$). Therefore, a detailed model of Q_T is considered. Now, by applying KCL at node d'_B, (10) is obtained. Similarly, applying KCL at the node d'_T with the approximation that $(dv_{gs}^T/dt) \ll (dv_{ds}^T/dt)$ and $(dv_{g's'}^T/dt) \ll (dv_{d's'}^T/dt)$, (9)[2] is obtained. Now, applying KVL in the power loop and across the inductor load with the approximations $v_{ds}^B \approx v_{d's'}^B$ and $v_{ds}^T \approx v_{d's'}^T$, (11) and (12) are obtained, respectively. (10)-(12) represents a set of coupled nonlinear differential equations and governs the dynamics during the partial hard turn-on transition of the complementary device.

By replacing the expression for i_{ch}^T from (9) in (8), (13) is obtained. By substituting (11)-(12) and by using (5), (13) is reduced to (14) where $i_{dc} \in (I_0, I_T)$ and $i_L \in (I_{L0}, I_{LT})$ for $\tau \in (0, T)$. Now, replacing the expression for i_{dc} from (9), (15) is obtained. Using (5) and (6), (15) can be written as (16)[3], where $C_{B(eq)}^{Er}$ and $C_{B(eq)}^{Q}$ are energy-equivalent and charge-equivalent capacitances. In (16), the first, second, and third terms represent the energy supplied by the DC bus, energy stored in the equivalent output capacitance of Q_B and change in stored energy in the parasitic inductance, respectively. Similarly, the fourth, fifth, and sixth term represents the energy

[1] $C_{B(eq)} = (C_{oss}(v_{ds}^B) + C_{ext} + C_{g'd'(e)}^B)$
[2] $C_{T(eq)} = (C_{oss}(v_{ds}^T) + C_{ext} + C_{g'd'(e)}^T)$
[3] $V^\alpha = V_{dc} - V^*$

$$E_{QT} = \int_0^T v_{ds}^T \left(i_{dc} - i_L - C_{T(eq)} \frac{d}{dt} v_{ds}^T \right) d\tau = \int_0^T v_{ds}^T i_{dc} d\tau - \int_0^T v_{ds}^T i_L d\tau + \int_0^{V^*} v_{ds}^T C_{T(eq)} dv_{ds}^T \tag{13}$$

$$= \left(V_{dc} \int_0^T i_{dc} d\tau - \int_0^T v_{ds}^B i_{dc} d\tau - (L_d + L_s) \int_{I_0}^{I_T} i_{dc} di_{dc} \right) - \left(V_o \int_0^T i_L d\tau - \int_{I_{L0}}^{I_{LT}} L i_L di_L \right) + \underbrace{\frac{1}{2} C_{T(eq)}^{Er}(0, V^*) V^{*2}}_{E_{oss}^T(V^*)} \tag{14}$$

$$= V_{dc} \int_{V_{dc}-V^*}^{V_{dc}} C_{B(eq)} dv_{ds}^B - \int_{V_{dc}-V^*}^{V_{dc}} C_{B(eq)} v_{ds}^B dv_{ds}^B - (L_d + L_s) \int_{I_0}^{I_T} i_{dc} di_{dc} - \left(V_o \int_0^T i_L d\tau - \int_{I_{L0}}^{I_{LT}} L i_L di_L \right) + E_{oss}^T(V^*) \tag{15}$$

$$= V_{dc} \left(V_{dc} - V^{\alpha} \right) C_{B(eq)}^Q (V^{\alpha}, V_{dc}) - \underbrace{\frac{1}{2} C_{B(eq)}^{Er}(V^{\alpha}, V_{dc})(V_{dc}^2 - (V^{\alpha})^2)}_{E_{oss}^B(V^{\alpha})} - \frac{1}{2}(L_d + L_s)(I_T^2 - I_0^2) - V_o \int_0^T i_L d\tau + \frac{1}{2} L \left(I_{LT}^2 - I_{L0}^2 \right) \tag{16}$$

$$+ E_{oss}^T(V^*)$$

TABLE I: Extracted device parameters form Datasheet for SiC MOSFET (LSIC1MO120E0080, Littelfuse)

V_{th} (V)	K_p (A/V^2)	K_f	θ $(1/V)$	P_{vf}	$R_{g(i)}$ (Ω)	C_{gs} (nF)	k_1 (nF)	k_2 (V)	k_3 (nF)	V_{td} (V)	k_4 (nF)	k_5 (V)	k_6 (nF)	k_7 (V)	k_8 (nF)	k_9 (V)
5.154	1.013	1.761	0.01	0.643	0.8	1.123	1.214	0.3716	0.8586	12	0.052	2.7589	1.233	2.57	2.347	0.85

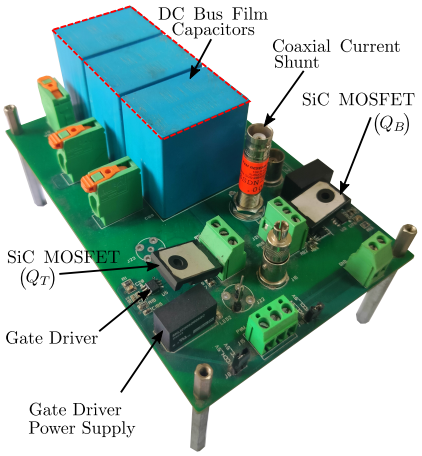


Fig. 5: Double Pulse Test Setup

delivered to the source V_o, energy delivered to the load, and energy stored in the equivalent output capacitance of Q_T.

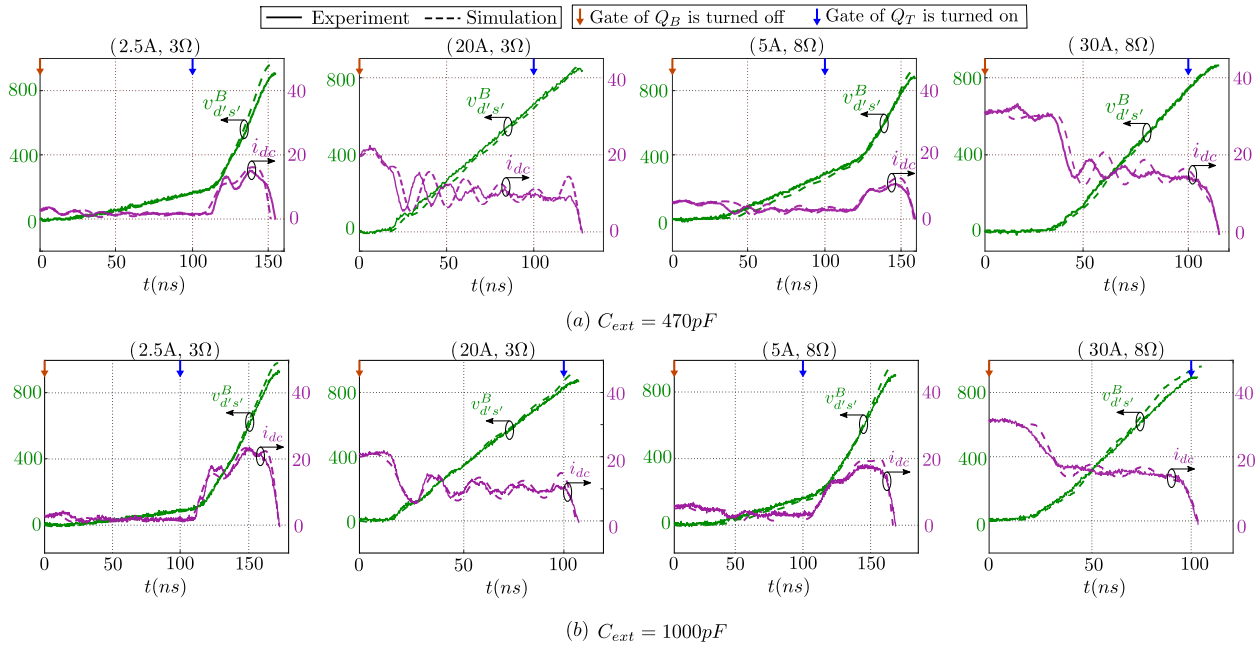
IV. Experimental Results and Discussion

Fig. 5 shows the double pulse test (DPT) setup used to capture the switching transients of SiC MOSFETs. The setup is rated for 800V input DC voltage and load current up to 35A. The DPT is conducted for a SiC MOSFET (LSIC1MO120E0080, 39A,1200V from Littelfuse) in a half-bridge configuration. By curve-fitting the datasheet curves (transfer characteristics, output characteristics, and capacitance vs vds plots) using (1)-(4), the device-related parameters are extracted and are shown in Table I. External circuit parasitics are extracted using [10]: $L_{dc} = 28.7nH$, $L_d = 10nH$, $L_s = 8.27nH$, $C_{g'd'(e)}^B = C_{g'd'(e)}^T = 5.4pF$. Gate drive with capacitor isolator Si8271 (Silicon lab), followed by a current booster IXDN609SI (IXYS), is used to drive the gate of the SiC MOSFET. Gate voltage levels are $V_{GG} = 20V$ and $V_{EE} = -5V$. The test conditions are: $V_{dc} = 800V$, $R_{g(e)} = 3, 8\Omega$, $C_{ext} = 470pF, 1000pF$ and $I_0 = 2.5, 5, 10, 15, 20, 25A$. This constitutes a total of 24 operating conditions. All the experiments were conducted at room temperature ($\approx 25°C$).

The drain-source voltage $v_{d's'}^B(t)$, device current $i_d(t)$ and load current $i_L(t)$ are the key waveforms. They are measured using a high-voltage differential probe (THDP0200) with 200 MHz bandwidth, a coaxial current shunt resistor (SSDN-414-10) from T&M Research, and a 120MHz ac/dc current probe (TCP0030), respectively. These signals are captured in a 1 GHz mixed-signal oscilloscope (MDO2104) from Tektronix and then processed in MATLAB. A deskew and calibration fixture (067-1686-00 from Tektronix) is used to match the delay of the current and voltage probes.

The behavioral model described in Section II was simulated in MATLAB/Simulink. In fig. 6, $v_{d's'}(t)$ and $i_{dc}(t)$ waveforms obtained from the behavioral simulation are compared with experiment for two values of external capacitance $C_{ext} = 470pF, 1000pF$ and for eight operating conditions. It can be observed that waveforms obtained from behavioral simulation in MATLAB/Simulink match closely with the DPT experiment. Thus, it can be concluded that the behavioral simulation is sufficiently accurate in capturing the partial hard turn-on dynamics of SiC MOSFET, and it can be used to estimate the partial hard turn-on loss of the complementary SiC MOSFET.

As evident from Fig. 6, partial hard turn-on of Q_T occurs for low-load currents, whereas it experiences soft turn-on for higher values of load currents. In Table III, partial hard turn-on loss estimated using (16) is compared with that obtained from the simulation for $C_{ext} = 470pF$ and $C_{ext} = 1000pF$ and large load variations. It can be observed that the proposed method predicts the loss in close agreement with the behavioral model. To estimate the partial hard turn-on loss from the experiment using (16), two example cases are shown in Table II.



(a) $C_{ext} = 470pF$

(b) $C_{ext} = 1000pF$

Fig. 6: Simulation and experimental waveforms ($V_{dc} = 800V$, $T_{dt} = 100ns$) (a) $C_{ext} = 470pF$ (b) $C_{ext} = 1000pF$

TABLE II: Calculation of E_{QT} from experiment using (16)

C_{ext} (pF)	$R_{g(e)}$ (Ω)	I_0 (A)	$C^Q_{B(eq)}(V_{dc}-V^*,V_{dc})$ (pF)	$C^{Er}_{B(eq)}(V_{dc}-V^*,V_{dc})$ (pF)	V^* (V)	I_0 (A)	I_T (A)	I_{L0} (A)	I_{LT} (A)	V_0 (V)	$E^T_{oss}(V^*)$ (μJ)	E_{QT} (μJ)
470	3	2.5	218.12	1889.15	596	1.818	11.716	3.12	3.2	0	104	171.24
1000	8	2.5	1143.46	1119.24	704	2.424	19.796	2.916	3.104	0	287	500.97

TABLE III: Comparison of E_{QT} estimated by proposed method with behavioral simulation

C_{ext} (pF)	E_{QT} (μJ)	$R_{g(e)} = 3\Omega$					$R_{g(e)} = 8\Omega$				
		2.5A	5A	10A	15A	20A	2.5A	5A	10A	15A	20A
470 pF	Simulation	182.95	75.66	1.4995	0	0	193.202	83.756	5.637	0.67	0
	Proposed	171.24	62.87	0	0	0	182.76	67.13	0.08	0	0
1000 pF	Simulation	461.87	258.15	87.558	12.129	1.536	512.39	302.47	142.52	42.107	6.145
	Proposed	456.17	276.49	100.90	19.64	0	500.97	320.80	111.46	19.73	0

V. Conclusion

This paper proposed an energy-based method to estimate the partial hard turn-on loss of the complementary SiC MOSFET in a soft-switching converter. The proposed method requires only the measurement of the active device's current and waveform along with the load current waveform to estimate the loss. It is validated using behavioral simulation for a 1200V SiC MOSFET for a wide range of operating conditions. The results presented in the paper show that the proposed method can estimate the partial hard turn-on loss sufficiently accurately ($\leq$ 7% error) at low current levels ($< 5A$). However, an increase in %error is observed at higher load currents where loss is very small.

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